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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/068,004	02/08/2002	Woo Young So	1514.1010	6442

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EXAMINER	
SEFER, AHMED N	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 06/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/068,004	SO ET AL.	
	Examiner	Art Unit	
	A. Sefer	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12,14-16,22,24 and 25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12,14-16,22,24 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment filed April 5, 2005 has been entered; no new claims have been introduced.

Response to Arguments

2. Applicant's arguments, see pages 6 and 11, filed 4/5/2005, with respect to claims 12 and 22 have been fully considered. While the arguments with respect to claim 12 are persuasive, the arguments with respect to claim 22 are not. The obviousness rejection of claim 12 has been withdrawn.

3. Applicants argue that the combined references of Yoneda ("Yoneda") USPN 5,837,568 in view of Yamazaki et al. US PG-Pub 2003/0207502 ("Yamazaki '502") and Yamazaki et al. ("Yamazaki") USPN 5,568,288/Teramoto et al. ("Teramoto") USPN 5,897,344 do not disclose all the claimed elements either explicitly or inherently. Specifically, Applicants argue that the low-density regions of Yoneda are not confined to the area under the sidewalls. Furthermore, Applicants argue that regions of 103 Yamazaki '502 are not located under spacers 109, but extend out under the gate electrode 107.

4. In response to Applicants argument that low-density regions of Yoneda are not confined to the area under the sidewalls, as stated in the previous Office Action the low-density regions are partially located under spacers and this deficiency is cured by Yamazaki '502. In Yamazaki '502 regions of 103 are located under spacers 109 (par. 0075).

5. In response to Applicants argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the

teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

6. Claims 12 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoneda in view of Yamazaki '502 and Yamazaki/Teramoto.

Yoneda discloses in figs. 12 and 13 a thin film transistor (TFT), comprising: a substrate 10; a semiconductor layer formed over said substrate having end portions; a first insulating layer 12 disposed on said semiconductor layer so as to expose ones of the end portions of said semiconductor layer; a gate electrode 13 formed over said first insulating layer; a capping layer 14 formed over said gate electrode; spacers 15 formed over said first insulating layer and on both sidewall portions of said gate electrode; high-density source and drain regions 11S/11D formed at the ones of the end portions of said semiconductor layer exposed beyond said spacers; low-density source and drain regions 11L having a same conductivity as high-density source and drain regions formed at regions of said semiconductor layer partially under spacers between the gate electrode and the high density source and drain regions, wherein said semiconductor layer has lightly doped drain (LDD) regions partially under said spacers; source and drain electrodes 17/18 which directly contact, respectively, said high density source and drain regions, but lacks anticipation of source and drain electrodes contacting high density source and drain regions without contact holes.

Yamazaki '502 discloses a thin film transistor (TFT), comprising: a substrate; a semiconductor layer 303/304 having end portions formed over said substrate; a first insulating layer 106/305 formed over said semiconductor layer so as to expose one of the end portions of said semiconductor layer; a gate electrode 107 formed over said first insulating layer; spacers 109 formed over said first insulating layer and on side wall portions of said gate electrode; high-density source and drain regions 104 formed at the ones of the end portions of said semiconductor layer exposed beyond said spacers; low-density source and drain regions 103 having a same conductivity as high-density source and drain regions formed at regions of said semiconductor layer under said spacers between the gate electrode and the high density source and drain regions, wherein said semiconductor layer has lightly doped drain (LDD) regions under said spacers; source and drain electrodes 115 which directly contact, respectively, said high density source and drain regions.

Yamazaki discloses in figs. 21 and 22 a thin film transistor (TFT), comprising: a substrate; a semiconductor layer formed over said substrate having end portions; a gate electrode 107 formed over an insulating layer 103; and source and drain electrodes 102 which directly contact, respectively, and without contact holes, high density source and drain regions 104/105. Similarly, Teramoto discloses in fig. 1D a thin film transistor (TFT), comprising: a substrate; a semiconductor layer formed over said substrate 11 having end portions; a gate electrode 15 formed over an insulating layer 12; and source and drain electrodes 23/24 which directly contact, respectively, and without contact holes, high density source and drain regions 17/19.

Therefore, in view of Yamazaki '502 and Yamazaki/Teramoto, one having ordinary skill in the art at the time the invention was made would be motivated to incorporate the teachings of

Yamazaki '502 since the spacers would function as masking layers. It would have been obvious to incorporate Yamazaki's/Teramoto's teachings since that would minimize source/drain sheet resistance and eliminate the need for performing mask alignment as taught by Teramoto.

Regarding claim 14, Yoneda discloses (col. 13, lines 10-14 and 29-35) said first insulating layer, said capping layer and said spacer are of an oxide.

7. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoneda in view of Kim et al. ("Kim") 6,706,569 and Yamazaki/Teramoto.

Yoneda discloses in figs. 12 and 13 a thin film transistor (TFT), comprising: a substrate 10; a semiconductor layer formed over said substrate having end portions; a first insulating layer 12 disposed on said semiconductor layer so as to expose ones of the end portions of said semiconductor layer; a gate electrode 13 formed over said first insulating layer; a capping layer 14 formed over said gate electrode; spacers 15 formed over said first insulating layer and on both sidewall portions of said gate electrode; high-density source and drain regions 11S/11D formed at the ones of the end portions of said semiconductor layer exposed beyond said spacers; low-density source and drain regions 11L having a same conductivity as high-density source and drain regions formed at regions of said semiconductor layer partially under spacers between the gate electrode and the high density source and drain regions, wherein said semiconductor layer has lightly doped drain (LDD) regions partially under said spacers; source and drain electrodes 17/18 which directly contact, respectively, said high density source and drain regions, but lacks anticipation of source and drain electrodes contacting high density source and drain regions without contact holes.

Kim discloses in fig. 11 a device comprising: a substrate; a semiconductor layer 1 having end portions formed over said substrate; a first insulating layer 65 formed over said semiconductor layer so as to expose one of the end portions of said semiconductor layer; a gate electrode 5 formed over said first insulating layer; a capping layer 6 over said gate electrode; spacers 69 formed over said first insulating layer and on side wall portions of said gate electrode; high-density source and drain regions 1s"/1d" formed at the ones of the end portions of said semiconductor layer exposed beyond said spacers; low-density source and drain regions 1s'/1d' having a same conductivity as high-density source and drain regions formed at regions of said semiconductor layer under said spacers between the gate electrode and the high density source and drain regions, and wherein said semiconductor layer has lightly doped drain (LDD) regions under said spacers.

Yamazaki discloses in figs. 21 and 22 a thin film transistor (TFT), comprising: a substrate; a semiconductor layer formed over said substrate having end portions; a gate electrode 107 formed over an insulating layer 103; and source and drain electrodes 102 which directly contact, respectively, and without contact holes, high density source and drain regions 104/105. Similarly, Teramoto discloses in fig. 1D a thin film transistor (TFT), comprising: a substrate; a semiconductor layer formed over said substrate 11 having end portions; a gate electrode 15 formed over an insulating layer 12; and source and drain electrodes 23/24 which directly contact, respectively, and without contact holes, high density source and drain regions 17/19.

Therefore, in view of Kim and Yamazaki/Teramoto, one having ordinary skill in the art at the time the invention was made would be motivated to incorporate Kim's teachings since the spacers would function as implantation masks as taught by Kim. It would have been obvious to

incorporate Yamazaki's/Teramoto's teachings since that would minimize source/drain sheet resistance and eliminate the need for performing mask alignment as taught by Teramoto.

8. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoneda in view of Kim and Yamazaki/ Teramoto.

Yoneda discloses in figs. 12 and 13 an active matrix display device, comprising: a substrate 10; a semiconductor layer having end portions formed over said substrate; a first insulating layer 12 formed over said semiconductor layer so as to expose one of the end portions of said semiconductor layer; a gate electrode 13 formed over said first insulating layer; a capping layer 14 formed over said gate electrode; spacers 15 formed over said first insulating layer and on side wall portions of said gate electrode and said capping layer; high-density source and drain regions 11formed at the ones of the end portions of said semiconductor layer exposed beyond said spacers; low-density source and drain regions having a same conductivity as said high-density source and drain regions formed at off-set regions of said semiconductor layer partially under said spacers so as to have said semiconductor layer with lightly doped drain (LDD) regions partially under said spacers; source and drain electrodes 17/18 which directly contact, respectively, said high density source and drain regions; a planarization layer 19 having an opening portion CT3 which exposes a portion of one of said source and drain electrodes; and a pixel electrode 20 formed on the planarization layer, the pixel electrode contacting one of the second source and drain electrodes through the opening portion, but lack anticipation of source and drain electrodes contacting high density source and drain regions without contact holes.

Kim discloses in fig. 11 a device comprising: a substrate; a semiconductor layer 1 having end portions formed over said substrate; a first insulating layer 65 formed over said semiconductor layer so as to expose one of the end portions of said semiconductor layer; a gate electrode 5 formed over said first insulating layer; a capping layer 6 over said gate electrode; spacers 69 formed over said first insulating layer and on side wall portions of said gate electrode; high-density source and drain regions 1s"/1d" formed at the ones of the end portions of said semiconductor layer exposed beyond said spacers; low-density source and drain regions 1s'/1d' having a same conductivity as high-density source and drain regions formed at regions of said semiconductor layer under said spacers between the gate electrode and the high density source and drain regions, and wherein said semiconductor layer has lightly doped drain (LDD) regions under said spacers.

Yamazaki discloses in figs. 21 and 22 a thin film transistor (TFT), comprising: a substrate; a semiconductor layer formed over said substrate having end portions; a gate electrode 107 formed over an insulating layer 103; and source and drain electrodes 102 which directly contact, respectively, and without contact holes, high density source and drain regions 104/105. Similarly, Teramoto discloses in fig. 1D a thin film transistor (TFT), comprising: a substrate; a semiconductor layer formed over said substrate 11 having end portions; a gate electrode 15 formed over an insulating layer 12; and source and drain electrodes 23/24 which directly contact, respectively, and without contact holes, high density source and drain regions 17/19.

Therefore, in view of Kim and Yamazaki/Teramoto, one having ordinary skill in the art at the time the invention was made would be motivated to incorporate Kim's teachings since the spacers would function as implantation masks as taught by Kim. It would have been obvious to

incorporate Yamazaki's/Teramoto's teachings since that would minimize source/drain sheet resistance and eliminate the need for performing mask alignment as taught by Teramoto.

9. Claim 22 and 25 rejected under 35 U.S.C. 103(a) as being unpatentable over Yoneda in view of Yamazaki '502 and Yamazaki/ Teramoto.

Yoneda discloses in figs. 12 and 13 an active matrix display device, comprising: a substrate 10; a semiconductor layer having end portions formed over said substrate; a first insulating layer 12 formed over said semiconductor layer so as to expose one of the end portions of said semiconductor layer; a gate electrode 13 formed over said first insulating layer; a capping layer 14 formed over said gate electrode; spacers 15 formed over said first insulating layer and on side wall portions of said gate electrode and said capping layer; high-density source and drain regions 11formed at the ones of the end portions of said semiconductor layer exposed beyond said spacers; low-density source and drain regions having a same conductivity as said high-density source and drain regions formed at off-set regions of said semiconductor layer partially under said spacers so as to have said semiconductor layer with lightly doped drain (LDD) regions partially under said spacers; source and drain electrodes 17/18 which directly contact, respectively, said high density source and drain regions; a planarization layer 19 having an opening portion CT3 which exposes a portion of one of said source and drain electrodes; and a pixel electrode 20 formed on the planarization layer, the pixel electrode contacting one of the second source and drain electrodes through the opening portion, but lack anticipation of source and drain electrodes contacting high density source and drain regions without contact holes.

Yamazaki '502 discloses in figs. 1-4 an active matrix display device, comprising: a substrate; a semiconductor layer 303/304 having end portions formed over said substrate; a first insulating layer 106/305 formed over said semiconductor layer so as to expose one of the end portions of said semiconductor layer; a gate electrode 107 formed over said first insulating layer; spacers 109 formed over said first insulating layer and on side wall portions of said gate electrode; high-density source and drain regions 104 formed at the ones of the end portions of said semiconductor layer exposed beyond said spacers; low-density source and drain regions 103 having a same conductivity as high-density source and drain regions formed at regions of said semiconductor layer under spacers between the gate electrode and the high density source and drain regions, wherein said semiconductor layer has lightly doped drain (LDD) regions under said spacers; source and drain electrodes 115 which directly contact, respectively, said high density source and drain regions.

Yamazaki discloses in figs. 21 and 22 a thin film transistor (TFT), comprising: a substrate; a semiconductor layer formed over said substrate having end portions; a gate electrode 107 formed over an insulating layer 103; and source and drain electrodes 102 which directly contact, respectively, and without contact holes, high density source and drain regions 104/105. Similarly, Teramoto discloses in fig. 1D a thin film transistor (TFT), comprising: a substrate; a semiconductor layer formed over said substrate 11 having end portions; a gate electrode 15 formed over an insulating layer 12; and source and drain electrodes 23/24 which directly contact, respectively, and without contact holes, high density source and drain regions 17/19.

Therefore, in view of Yamazaki '502 and Yamazaki/Teramoto, one having ordinary skill in the art at the time the invention was made would be motivated to incorporate the teachings of

Yamazaki '502 since the spacers would function as masking layers. It would have been obvious to incorporate Yamazaki's/Teramoto's teachings since that would minimize source/drain sheet resistance and eliminate the need for performing mask alignment as taught by Teramoto.

Regarding claim 25, Yamazaki '502 discloses (par. 0343 and fig. 25) an organic electro-luminescence (EL) layer 4029 and a cathode electrode 4030 sequentially formed on a first predetermined area of a pixel electrode and on a second predetermined area of a planarization layer 4142.

10. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoneda in view of Yamazaki '502 and Yamazaki/Teramoto as applied to claim 12 above and further in view of Yamazaki et al. (JP 11-261076) ("Yamazaki '076).

The combined references disclose the device structure as recited in the claim, but do not disclose a silicide layer.

Yamazaki '076 discloses in fig. 1 a silicide layer 105a or a refractory metal (as in claim 16) formed between said source electrode and said high-density source region and between said drain electrode and said high-density drain region.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate Yamazaki '076 with the device of the combined references, since that would lessen the source/drain regions in sheet resistance as taught by Yamazaki '076.

11. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoneda in view of Yamazaki '502 and Yamazaki/Teramoto as applied to claim 22 above and further in view of Yamazaki '076.

The combined references disclose the device structure as recited in the claim, but do not disclose a silicide layer.

Yamazaki '076 discloses in fig. 1 a silicide layer 105a or a refractory metal (as in claim 16) formed between said source electrode and said high-density source region and between said drain electrode and said high-density drain region.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate Yamazaki '076 with the device of the combined references, since that would lessen the source/drain regions in sheet resistance as taught by Yamazaki '076.

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (571) 272-1921.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANS
June 20, 2005